

FIG.1

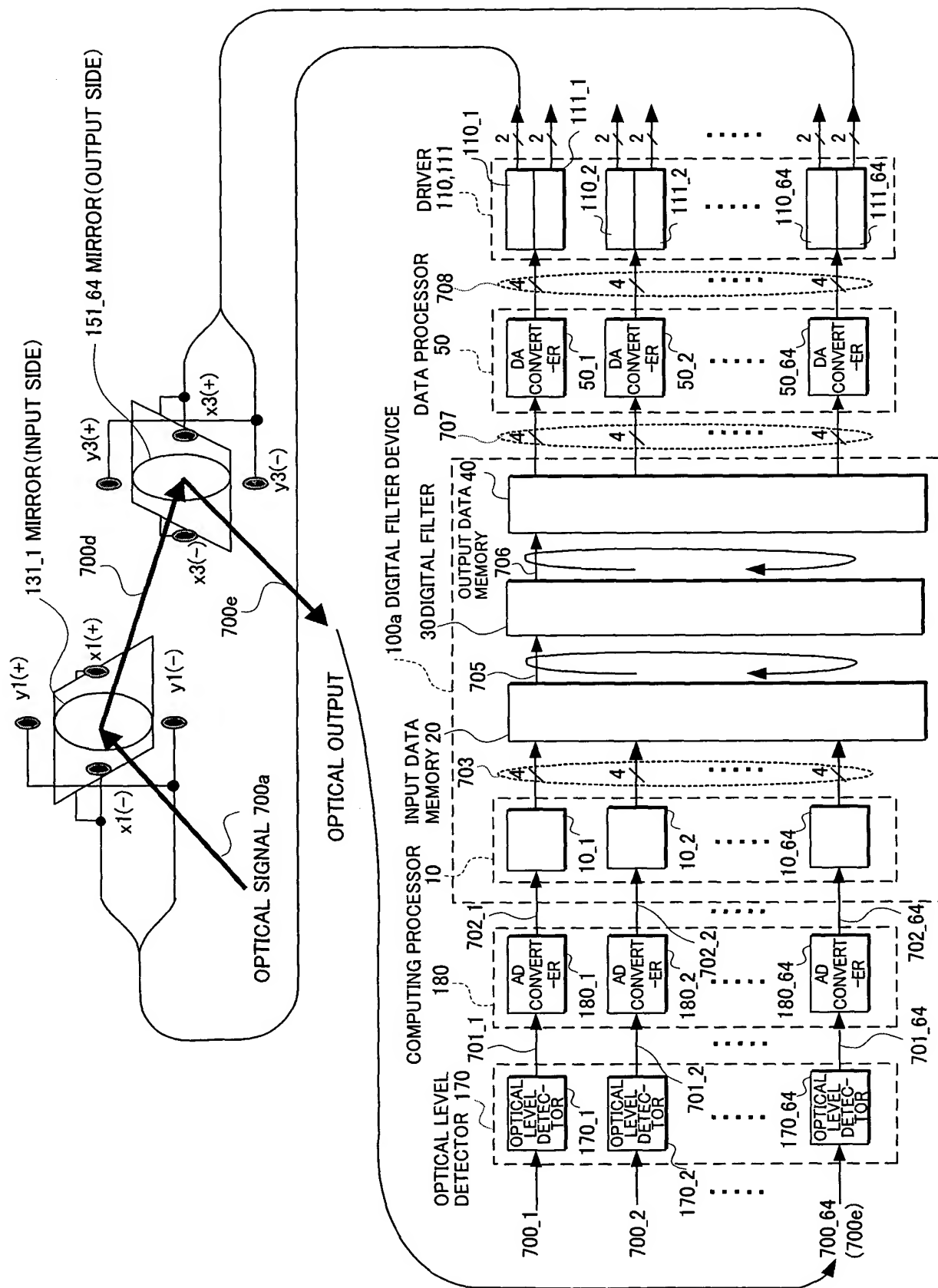


FIG.2

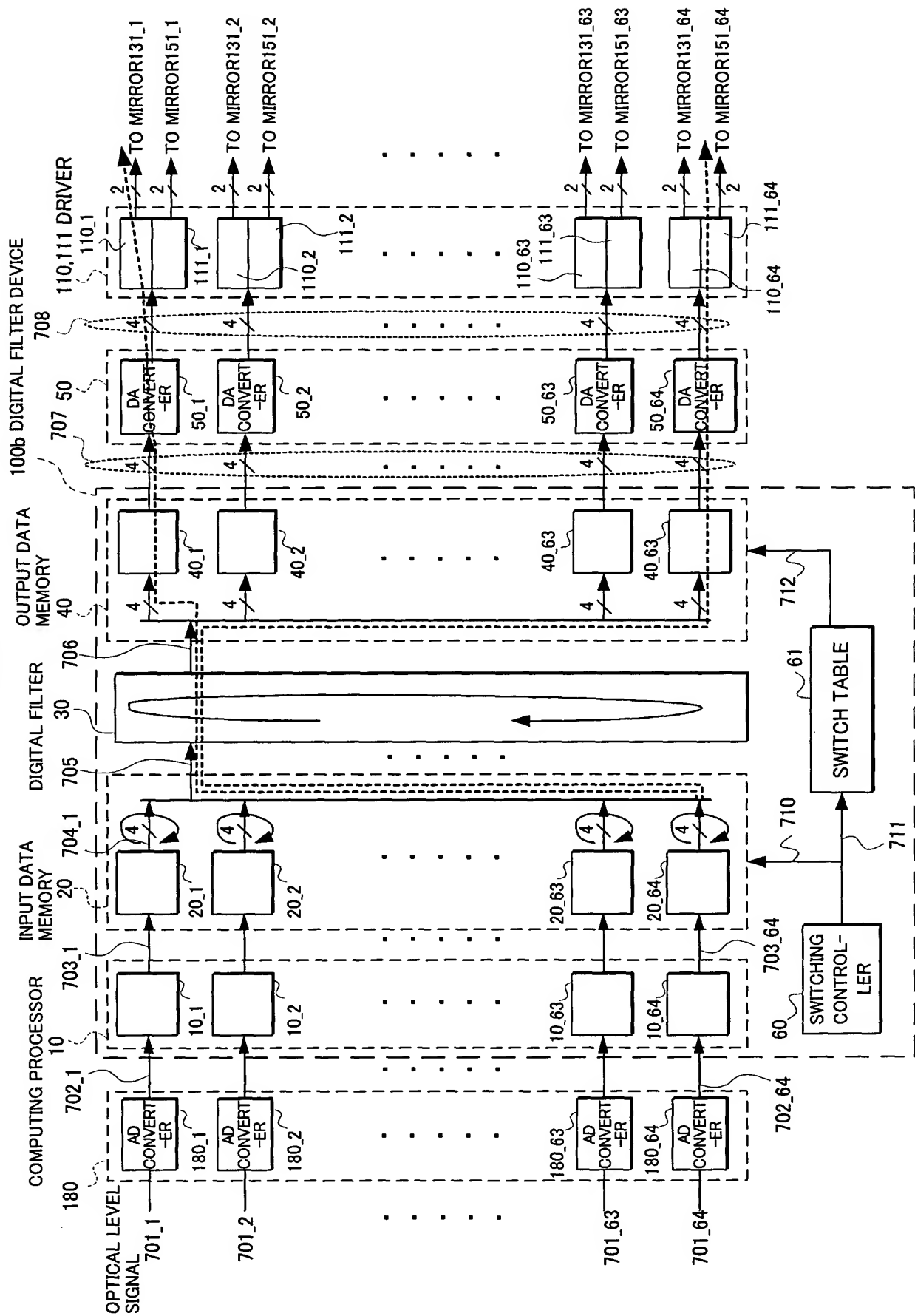


FIG.3

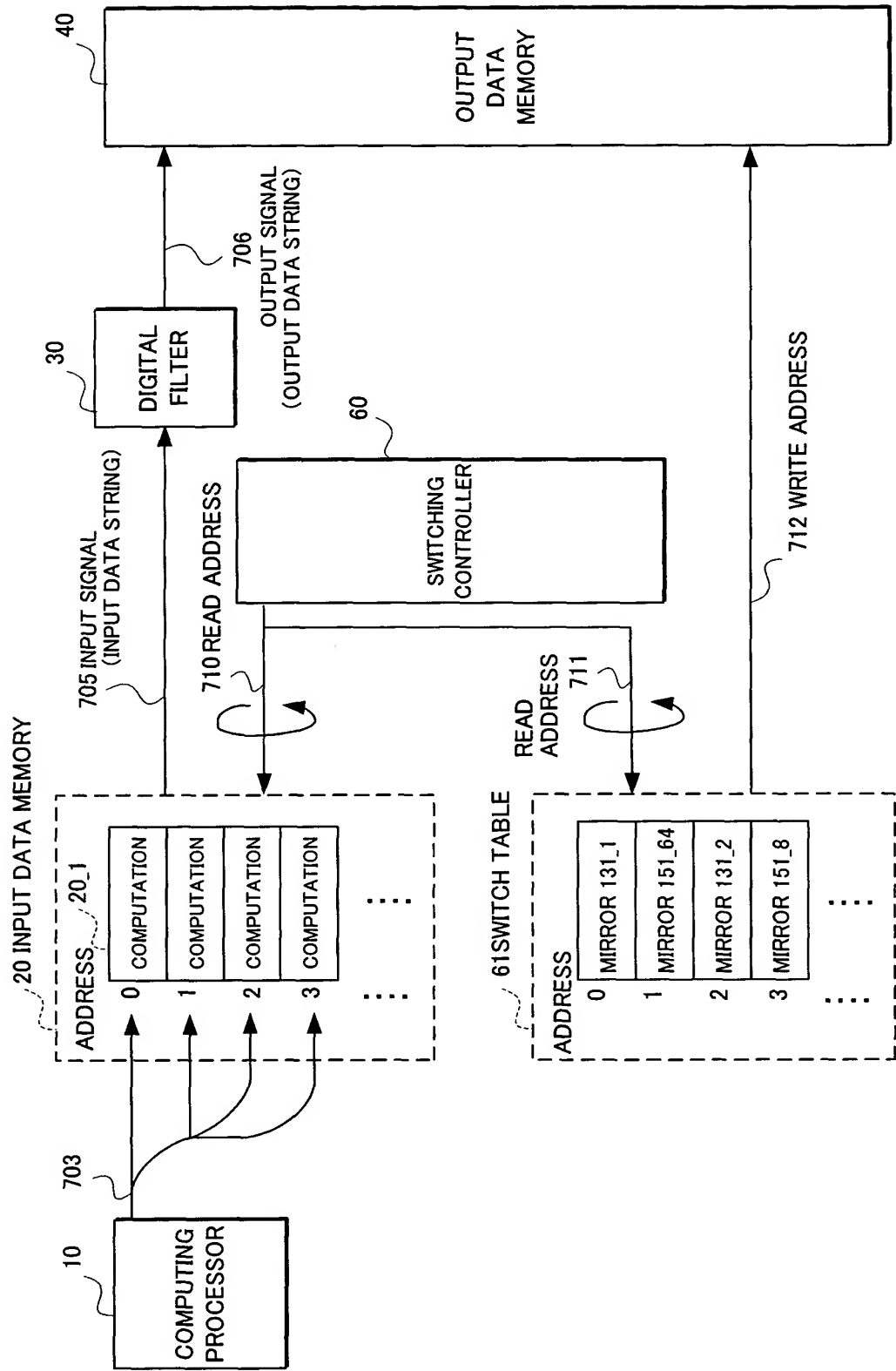


FIG.4A

PROCESSING CYCLE  
ADDRESS 710  
(INPUT DATA MEMORY  
READ ADDRESS)

ADDRESS 0	ADDRESS 1	ADDRESS 2	ADDRESS 3	ADDRESS 4	ADDRESS 5	ADDRESS 6	ADDRESS 7
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FIG.4B

SWITCH TABLE READ  
ADDRESS 711

0	1	2	3	4	5	6	6
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FIG.4C

SWITCH TABLE DATA 712  
(OUTPUT DATA MEMORY  
WRITE ADDRESS)

MIRROR 131_1	MIRROR 151_64	MIRROR 131_2	MIRROR 151_8	...	...	...	...
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FIG.4D

FILTER MEMORY  
WRITE ADDRESS 713  
READ ADDRESS 714

MIRROR 131_1	MIRROR 151_64	MIRROR 131_2	MIRROR 151_8	...	...	...	...
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FIG.4E

WRITE DATA 715 OF  
FILTER MEMORY

DATA- UNDER- CALCULATION FOR MIRROR 131_1	DATA- UNDER- CALCULATION FOR MIRROR 151_64	DATA- UNDER- CALCULATION FOR MIRROR 131_2	DATA- UNDER- CALCULATION FOR MIRROR 151_8	...	...	...	...
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FIG.4F

READ DATA 716 OF  
FILTER MEMORY

LAST DATA- UNDER- CALCULATION FOR MIRROR 131_1	LAST DATA- UNDER- CALCULATION FOR MIRROR 151_64	LAST DATA- UNDER- CALCULATION FOR MIRROR 131_2	LAST DATA- UNDER- CALCULATION FOR MIRROR 151_8	...	...	...	...
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FIG.5

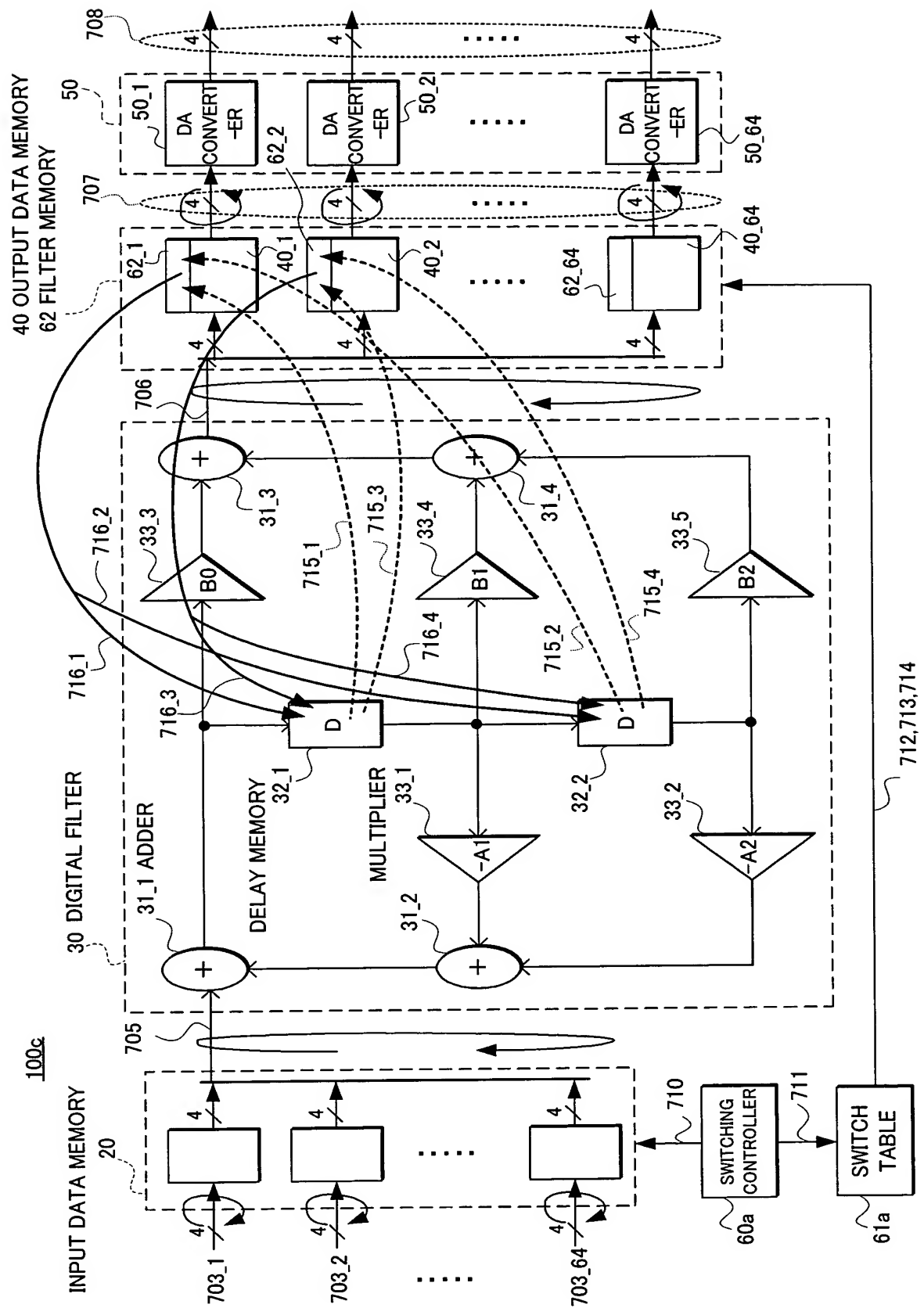




FIG.7  
PRIOR ART

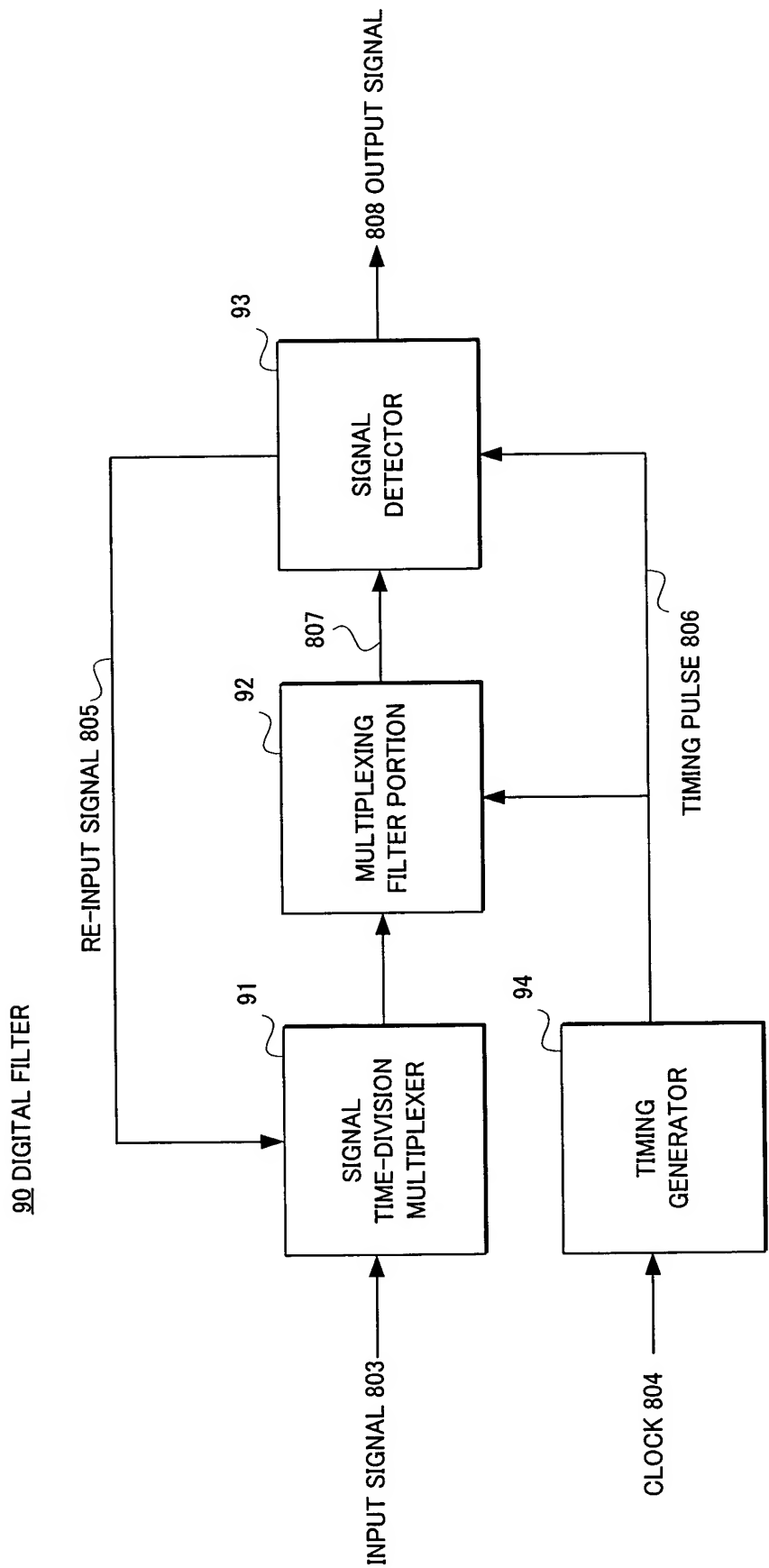


FIG.8  
PRIOR ART

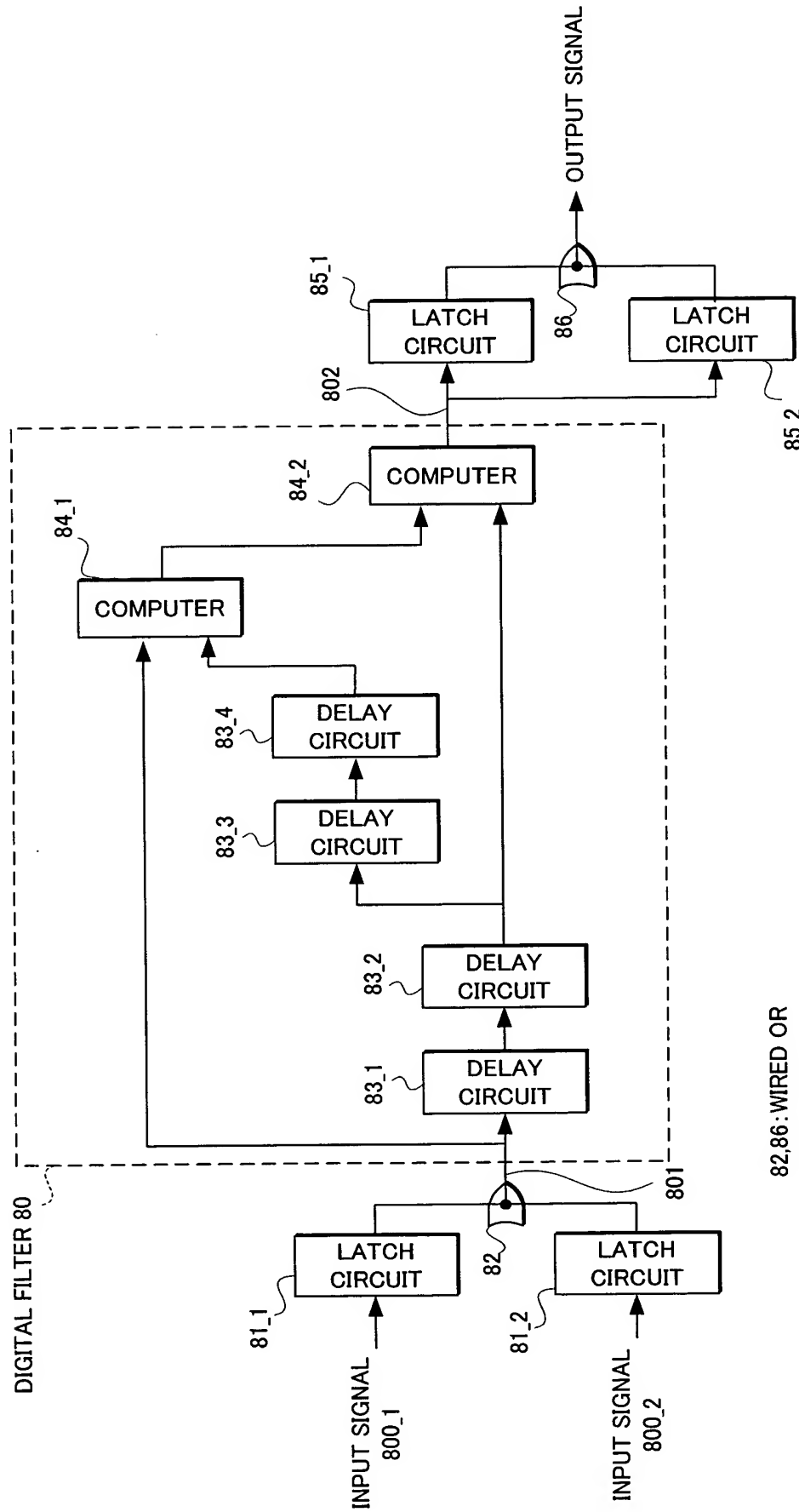




FIG.9

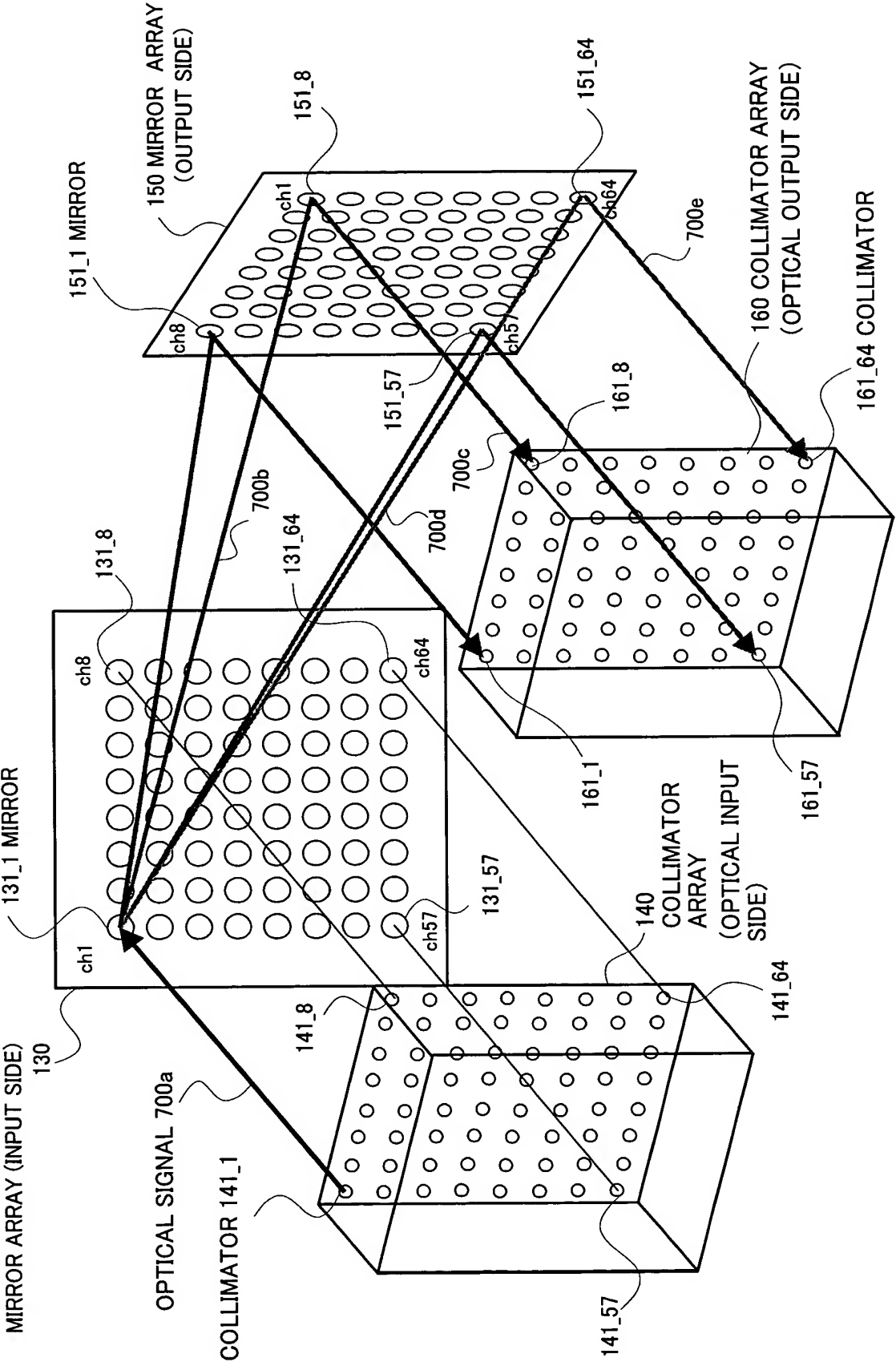


FIG.10

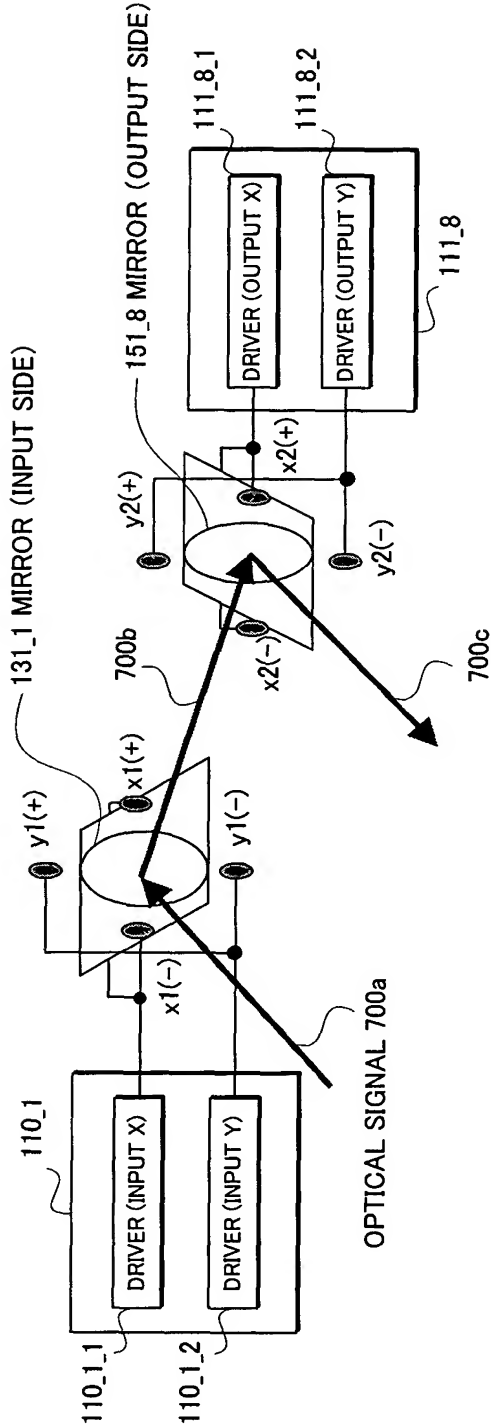


FIG.11  
PRIOR ART

